Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

IN THE TITLE:

The title has been changed to:

--PARALLEL PULSE SIGNAL PROCESSING APPARATUS WITH PULSE SIGNAL PULSE COUNTING GATE, PATTERN RECOGNITION APPARATUS, AND IMAGE INPUT APPARATUS--

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance: claims 1-12, 14-22, and 24 are considered allowable since when reading the claims in light of the specification, as per MPEP §2111.01 or Toro Co. v. White Consolidated Industries Inc., 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999), none of the references of record alone or in combination disclose or suggest the combination of limitations specified in the independent claims, specifically a pulse output means for

outputting a pulse signal on a basis of a result of the modulation processing, and wherein said gate circuit counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection elements, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number as essentially disclosed in independent claims 1, 7, 8, 9, 10, and 18-22 of the instant application (as defined at e.g., pg. 4 and 24-25 of the specification of the instant application).

3. A practical application for the invention is disclosed on page 3: "The present invention…has as its object to solve the wiring problems and reduce the circuit scale and power consumption" of neural network based circuitry for image signal processing.

4. A computer readable medium for the claimed parallel pulse signal processing apparatus has been interpreted as being a tangible computer memory such as "a floating gate element…or a digital memory (e.g., SRAM or MRAM)" (as disclosed at p. 37).

The Prior art of reference *Matsugu*, "Hierarchical Pulse-coupled Neural Network Model with Temporal Coding and Emergent Feature Binding Mechanism", 2001 discloses a parallel pulse signal processing including a plurality of pulse output arithmetic, a plurality of connection elements which parallelly connect predetermined elements of the arithmetic elements, and a gate circuit which selectively passes pulse signals from the plurality of connection elements, characterized in that said arithmetic element comprises input means for inputting a plurality of time series pulse signals, modulation processing means for executing predetermined modulation processing on the basis of the plurality of time series pulse signals which are input, and pulse output means for outputting a pulse signal on the basis of a result of modulation processing, and said gate circuit selectively passes, of the signals from said plurality of connection elements, a finite number of pulse signals corresponding to predetermined upper output levels.

Matsugu does not teach a pulse output means for outputting a pulse signal on a basis of a result of the modulation processing, and wherein said gate circuit counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection

elements, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number as specified in the independent claims of the instant application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

/Nathan H. Brown, Jr./
Examiner, Art Unit 2129

/David R Vincent/
Supervisory Patent Examiner, Art Unit 2129